O.P.Code:23EC0447 | R23 | H.T.No.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech. III Year I Semester Regular Examinations December-2025

DIGITAL CIRCUITS

(Electrical & Electronics Engineering)

Time: 3 Hours **Max. Marks: 70**

PART-A

(Answer all the Questions **10 x 2 = 20** Marks)

1	a	State De-Morgan's theorem.	CO1	L1	2M
	b	Simplify the following Boolean expression into one literal. W'X (Z'+YZ) + X (W+Y'Z).	CO2	L2	2M
	c	Determine the Boolean expression for a half adder and full adder.	CO2	L1	2M
	d	Convert the binary number 1011 into Gray code.	CO3	L1	2M
	e	Define a decoder and mention one of its applications.	CO4	L1	2M
	f	State the difference between multiplexer and demultiplexer.	CO4	L1	2M
	g	Draw the truth table of an SR latch.	CO5	L1	2M
	h	Why is the master-slave configuration used in JK flip-flops?	CO5	L1	2M
	i	Write the difference between PROM and PLA.	CO6	L1	2M
	j	Mention two applications of ROM.	CO6	L1	2M

PART-B

(Answer all Five Units **5 x 10 = 50** Marks)

UNIT-I

2	a	State and prove the De-Morgan's Theorem with truth tables.	CO1	L3	5M
	b	State and prove the Consensus theorem.	CO1	L3	5M
		OR			
3	a	Simplify the following expression using the K-map for the 3-variable. Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'	CO1	L3	5M
	b	Simplify the following Boolean expressions using K-map. F(A, B, C, D)= Σm(1,3,7,11,15)	CO1	L3	5M

UNIT-II

4	a	Design & implement Half Adder with truth table.	CO3	L3	5M
	b	Design & implement Full Adder with truth table.	CO3	L3	5M
		OR			
5		Explain the concept of BCD addition and design a BCD adder circuit.	CO3	L2	10M

UNIT-III

6		Minimize the function F(A, B, C, D) = Σ m(1, 3, 4, 11, 12, 13, 14, 15) and implement it using an 8-to-1 multiplexer.	CO4	L2	10M
		OR			
7	a	Implement the following function F(A,B,C)=Σm(1,3,5,6) using16:1 MUX	CO4	L2	5M
	b	Implement the following function F(A,B,C)=Σm(1,3,5,6) using 8:1 MUX	CO4	L2	5M

UNIT-IV

8		Design a D flip-flop. Explain its truth table and applications.	CO5	L3	10M
		OR			
9		Distinguish between level triggered and edge triggered flip-flops with diagrams.	CO5	L2	10M

UNIT-V

10		Compare three combinational circuits: PLA, PAL and PROM.	CO6	L3	10M
		OR			
11		Implement PLA circuit for the following functions $F_1(A,B,C)$= Σm(3,5,6,7), $F_2(A,B,C)$= Σm(0,2,4,7).	CO6	L2	10M

*** END ***